Assignee: Intel Corporation
Docket No.: 2207/7942

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS	:	Deborah T. Marr, et al.
SERIAL NO.	:	09/490,172
FILED	:	January 22, 2000
FOR	:	ESTABLISHING THREAD PRIORITY IN A PROCESSOR OR THE LIKE
GROUP ART UNIT	:	2171
EXAMINER	:	Susan (Te Y.) Chen

M/S: APPEAL BRIEF - PATENT
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

REPLY BRIEF

Dear Sir:

This Reply Brief is filed in response to the Examiner's Answer of May 18, 2007.

ARGUMENT

The pending claims each require two values to be used in assigning priority between threads. For example, claim 1 uses a first value to indicate which of the threads has the higher priority and loads a counter with a second, predefined value, which is selected by control logic depending on the priority assigned to each thread. The counter is used in the allocating of priority between threads.

As stated in the Examiner's Answer, the primary reference, Kimura fails to disclose a counter loaded with a predetermined value by control logic, where the counter value is selected depending on the priority assigned, and the counter is used to allocate the resource between a plurality of threads. (pg. 4). It is assumed that the Examiner's Answer is referring to U.S. Patent No. 6,105,127 to Kimura. That patent does not describe a Task Priority Register or TPR. Neither term appears in the reference. Col. 8, line 59 to Col. 9, line 8 et seq. refers to a Priority Designating Register or PRI. This register includes two-bit fields that define the priority level for each logical processor (i.e., high, medium, and low; Col. 9, lines 36-42). An "inc pri" instruction is provided to raise the priority level for a logical processor. Col. 9, lines 48-50. As an example, a first logical processor can have a high priority level of "11"; a second logical processor can have a medium priority level of "10"; and a third logical processor can have a low priority level of "01". Each of these two-bit values would be stored in the PRI. The "inc pri" (or corresponding "dec pri") instruction would be used to change the priority level for each logical processor. Again, as indicated by the Final Office Action and the Examiner's Action, the Kimura reference does not disclose the counter and associated features recited in the pending claims.

Olarig does not make up for the deficiencies of Kimura. Olarig is providing almost the same functionality as Kimura – a two-bit value assigned to each processing unit to indicate the relative priority of one processing unit to the others. The difference lies in that instead of an instruction to increment or decrement the two-bit value, the two-bit value is incremented automatically each time an I/O interrupt is received. In essence, the two-bit value represents four priority levels for the four processing units. It is important, though, in Olarig, that each value be different, but otherwise, the value that is stored is random. The Examiner's Answer states that "Olarig further clearly discloses that the contents of the task priority register and the counter size is appended to a task priority register corresponding with a particular processing unit." It is noted that the size of the counter is set based on the number of processing units (see Col. 3, lines 52-55). Thus, if eight processing units are provided, then the width of the counter would be three bits so that a unique binary number can be provided to represent each of the processing units.

Since Kimura provides a two-bit value to indicate relative priority and instructions for changing that priority, there simply cannot be any teaching in the references to add the two-bit counters of Olarig to Kimura. At best, one skilled in the art given these two references would replace the two-bit priority level fields of Kimura with the two-bit counters of Olarig to indicate which logical processor has highest priority. Doing so provides a change in priority in a round robin fashion. Of course, given that Kimura provides instructions to increment and decrement the priority levels for each of the logic processors, coding could be provided to achieve the same result of round robin assignment of priority.

As stated above, the claimed invention provides more than a value to indicate priority, it provides a counter that is loaded with a predefined value, which is selected by control logic depending on the priority assigned to each thread. The value stored in the two-bit counter of

Olarig must be set up at initialization to insure that the four two-bit values are each different. Otherwise, more than one processing unit will determine that it has highest priority, which is undesirable. Thus the values that are initially stored in the two-bit counters of Olarig are based on an identification of the processing unit (e.g., processing unit number "1" or "01"). Since these values are based on an identification of the processing unit and could even be random, it cannot be said that the value stored in these counters is "depending on the priority assigned to each thread" as required by the claims.

Appellants reiterate the arguments presented in the Appeal Brief of January 16, 2007. In view of the arguments therein and those presented above, Appellants respectfully request that the rejection of claims 1, 3-11 and 13-20 under 35 U.S.C. § 103(a) be reversed.

CONCLUSION

Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 1, 3-11, and 13-21 under 35 U.S.C. § 103(a) direct the Examiner to pass the case to issue.

The Commissioner is hereby authorized to charge any additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon Deposit Account No. 11-0600. A copy of this sheet is enclosed for that purpose.

Respectfully submitted,

Date: July 18, 2007

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